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EXAMINER	
NGUYEN, LONG T	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 03/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/811,456	ISODA, MASAHITO	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *19-30,33-35,38-51,54-56,58 and 59* is/are allowed.

6)☐ Claim(s) *31,32,36,37,52,53 and 57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/479,927.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The amendment filed on 1/20/04 has been received and entered in the case.

2. In this office action, claims 31, 32, 36, 37 52, 53 and 57 are rejected under 35 U.S.C. 112, 2nd paragraph, due to the amendment of independent claims.

Claim Objections

3. Claim 57 is objected to because of the following informalities: on line 2, it appears that "from enabled one" should be changed to --from the enabled--. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 31, 32, 36, 37, 52, 53 and 57 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to claim 31, the recitation "wherein each of the first and second circuit includes: an inverter, a PMOS transistor ...; and an NMOS transistor" recited on lines 2-7 are indefinite because it is not clear whether the inverter in the second circuit recited in claim 31 is the same as the inverter of the second circuit recited in independent claim 28; and whether the PMOS or the NMOS recited in claim 31 is the same as the MOS transistor of the second circuit recited in claim 28.

Claim 32 is indefinite because it includes the indefiniteness of claim 31. Further, the recitations "the NMOS transistor of the second circuit" recited on line 4 and "the PMOS transistor of the second circuit" recited on lien 5 are indefinite for the similar reason as discussed in claim 31.

Claims 36 and 37 are indefinite for the similar problems as discussed in claims 31 and 32 above.

Claims 52 and 53 are indefinite for the similar problems as discussed in claims 31 and 32 above.

With respect to claim 57, the recitation "an output signal from enabled one of the differential amplifier circuit and the second circuit" is unclear antecedent basis because it is not clear whether the "output signal" of the differential amplifier in the phrase is the same signal as the "amplified signal" (recited on line 3-4 and line 6-7 of independent claim 19).

Allowable Subject Matter

6. Claims 19-30, 33-35, 38-51, 54-56, 58 and 59 are allowed.

Claim 19, as amended, are allowed because the prior art of record fails to disclose or suggest an input buffer circuit including, in combination with other limitations, a second circuit including an inverter and a MOS transistor, and a control circuit for selectively enabling one of the differential amplifier circuit and the second circuit in accordance with a control signal while isolating the other one of the differential amplifier and the second circuit from at least one of the first power supply and the second power supply with the recited connections and operations set forth therein.

Claims 20, 21, 48, and 54-56 are allowed because they depend on claim 19.

Claim 22, as amended, are allowed because the prior art of record fails to disclose or suggest an input buffer circuit including, in combination with other limitations, a second circuit including an inverter and a MOS transistor, and a control circuit for selectively enabling one of the differential amplifier circuit and the second circuit in accordance with a control signal, wherein the control circuit enables the differential amplifier circuit and disable the second circuit when the first and second input signals have amplitudes smaller than a predetermined voltage.

Claims 23 and 24 are allowed because they depend on claim 22.

Claim 25, as amended, are allowed because the prior art of record fails to disclose or suggest an input buffer circuit including, in combination with other limitations, a second circuit including an inverter and a MOS transistor, and a control circuit for selectively enabling one of the differential amplifier circuit and the second circuit in accordance with a control signal, wherein the control circuit disables the differential amplifier circuit and enables the second circuit when the first and second input signals have amplitudes greater than a predetermined voltage.

Claims 26 and 27 are allowed because they depend on claim 22.

Claim 28, as amended, are allowed because the prior art of record fails to disclose or suggest an input buffer circuit including, in combination with other limitations, a second circuit including an inverter and a MOS transistor, and a control circuit for selectively enabling the differential amplifier circuit and the first and second circuits in accordance with a control signal, wherein the differential amplifier circuit and the first circuit are enabled and the second circuit is disabled when the first and second input signals have amplitudes smaller than a predetermined voltage.

Claims 29, 30 and 49-51 are allowed because they depend on claim 28.

Claim 33, as amended, are allowed because the prior art of record fails to disclose or suggest an input buffer circuit including, in combination with other limitations, a second circuit including an inverter and a MOS transistor, and a control circuit for selectively enabling the differential amplifier circuit and the first and second circuits in accordance with a control signal, wherein the differential amplifier circuit and the first circuit are disabled and the second circuit is enabled when the first and second input signals have amplitudes greater than a predetermined voltage.

Claims 34 and 35 are allowed because they depend on claim 33.

Claim 38, as amended, are allowed because the prior art of record fails to disclose or suggest an input buffer circuit including, in combination with other limitations, a second circuit including an inverter and a MOS transistor, and a control circuit for selectively enabling the differential amplifier circuit and one of the first circuit and the second circuit in accordance with a control signal while isolating the other one of the first circuit and the second circuit from the first power supply or the second power supply.

Claims 39-42, 58 and 59 are allowed because they depend on claim 38.

Claim 43, as amended, are allowed because the prior art of record fails to disclose or suggest an input buffer circuit including, in combination with other limitations, a second circuit including an inverter and a MOS transistor, and a control circuit for selectively enabling the differential amplifier circuit and the second circuit in accordance with a control signal and disabling the other one of the differential amplifier circuit and the second circuit.

Claim 44, as amended, are allowed because the prior art of record fails to disclose or suggest an input buffer circuit including, in combination with other limitations, a second circuit including an inverter and a MOS transistor, and a control circuit for selectively isolating one of the differential amplifier circuit and the second circuit from at least one of the first power supply and the second power supply while enabling the other one of the differential amplifier circuit and the second circuit.

Claim 45, as amended, are allowed because the prior art of record fails to disclose or suggest an input buffer circuit including, in combination with other limitations, a second circuit including an inverter and a MOS transistor, and a control circuit for selectively enabling one of the differential amplifier circuit and the second circuit in accordance with a control signal while isolating the other one of the differential amplifier circuit and the second circuit form at least one of the first power supply and the second power supply.

Claim 46, as amended, are allowed because the prior art of record fails to disclose or suggest an input buffer circuit including, in combination with other limitations, a second circuit including an inverter and a MOS transistor, and a control circuit for selectively enabling one of the differential amplifier circuit and the second circuit in accordance with a control signal and disabling the other one of the differential amplifier circuit and the second circuit.

Claim 47, as amended, are allowed because the prior art of record fails to disclose or suggest an input buffer circuit including, in combination with other limitations, a second circuit including an inverter and a MOS transistor, and a control circuit for selectively isolating one of the differential amplifier circuit and the second circuit from at least one of the first power supply

and the second power supply while enabling the other one of the differential amplifier circuit and the second circuit.

Response to Arguments

7. Applicant's arguments filed on 1/20/04 have been fully considered. Note that 19-30, 33-claims 35, 38-51, 54-56, 58 and 59 are now allowed. Also note that the amendment filed on 1/20/04 (amended independent claims) causes dependent claims 31, 32, 36, 37 52, 53 and 57 indefinite and are rejected under 35 U.S.C. 112, 2nd paragraph as discussed above.

Conclusion

8. In view of the 112 problems noted above, the allowability cannot be indicated to claims 31, 32, 36, 37 52, 53 and 57 at this time. However, if amended to overcome the indefinite problems, these claims would be allowed because they depend on allowable claims.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (703) 872-9306.

Any inquiry of general nature or relating to the status of this application or proceeding should be directed to the group receptionist whose telephone number is (703) 308-0956.

March 17, 2004

Long Nguyen
Art Unit: 2816